Rejection to the claims under 35 U.S.C. § 112, ¶2

Regarding the rejection under 35 U.S.C. § 112, second paragraph, of claims 1, 6-8, 10 and 15-20, Applicants respectfully traverse the Examiner's assertion that the recitation "a third wiring arranged in an outermost peripheral region of the chip and serving to connect the other end of the first wiring to an I/O slot different from the first I/O slot" is "not shown in the applicant's invention." The Examiner alleges that Fig. 1 shows third wiring 24 does not connect with the other end of the first wiring 14 and characterizes the first wiring as ending in via 15. Applicants disagree with the Examiner's characterization and conclusions.

Claim 1 recites, in part, a third wiring "serving to connect the other end of the first wiring to an I/O slot different form the first I/O slot." As shown in Fig. 2, for example, first wiring 14 connects to rewiring 21 by via 15, and rewiring 21 connects to third wiring 24 by vias 22 and 23. In this way, third wiring 24 serves to connect first wiring 14 to an I/O slot different from the first I/O slot. Thus, Fig. 2 shows a third wiring "serving to connect the other end of the first wiring to an I/O slot different from the first I/O slot," so that the claimed feature corresponds to an embodiment in Applicant's specification. Accordingly, the rejection under 35 U.S.C. § 112, second paragraph of claims 1, 6-8, 10 and 15-20 should be withdrawn.

Rejection under 35 U.S.C. § 103(a)

To establish a *prima facie* case of obviousness under 35 U.S.C. §103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element recited in the claims. (See M.P.E.P. §2143.03 (8th ed. 2001)). Second, there must be some suggestion or

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motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must "be found in the prior art, and not be based on applicant's disclosure." (M.P.E.P. §2143 (8th ed. 2001)).

Regarding the rejection under 35 U.S.C. §103(a) of claims 1, 6-8, 10 and 15-20, claim 1 recites a combinational including, at least, "a first pad arranged on a wiring level different from said first I/O slot and arranged above the first I/O slot without being connected to the first I/O slot."

In contrast, Applicants' so-called admitted prior art (Fig. 4) discloses a first pad 12a connected to the first slot 11a. Further, the specification for the present application describes at page 3, lines 3-5, that "[t]he pad 12a is connected to the I/O slot 11a [i.e., the first slot] via a wiring 14 and a via 15." Thus, Applicants' so-called admitted prior art does not teach or suggest at least a first pad "arranged above the first I/O slot without being connected to the first I/O slot," as recited in claim 1.

In contrast, in the exemplary embodiment of Fig. 2 of the present application a first pad 12a is arranged above the first I/O slot 11a without being connected to the first I/O slot. Particularly, a third wiring 24 "serv[es] to connect the other end of the first wiring to an I/O slot different from the first I/O slot."

Janai fails to cure the deficiencies of Applicants' so-called admitted prior art. Janai discloses a customizable three metal layer gate array device. A plurality of fusible links interconnect a plurality of transistors into an inoperable integrated circuit blank. Further, removing some of the fusible links renders the circuit blank into an operable

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gate array device. (See Abstract.) Thus, Janai relates to forming a gate array device, whereas the present application relates to making use of a pad in an integrated semiconductor circuit. (See page 1, lines 11-13 of the present application.) Because of this difference, Janai makes no reference to a pad. Accordingly, Janai does not disclose or suggest (nor does the Examiner allege that Janai discloses) at least a structure wherein a first pad is "arranged above the first I/O slot without being connected to the first I/O slot," as recited in claim 1.

Because a combination of Applicants' so-called admitted prior art and Janai does not teach or suggest at least the claimed first pad, the § 103(a) rejection of claim 1 should be withdrawn. Further reasons supporting patentability of claim 1 are provided below.

The Examiner admits at page 3 of the Office Action that Applicants' so-called admitted prior art does not disclose the claimed third wiring.

Janai also fails to teach or suggest the claimed third wiring. Particularly, Janai discloses vertical metal strips M2 that overlay the M1 layer (col. 2, line 58). As shown in Fig. 1A of Janai, vertical metal strips M2 are not "arranged in an outermost peripheral region of the chip," as recited in claim 1. Because a combination of Applicants' so called admitted prior art and Janai does not teach or suggest at least the claimed third wiring, the § 103(a) rejection of claim 1 should be withdrawn.

Additionally, by arranging the first pad "above the first I/O slot without being connected to the first I/O slot," and having a third wiring "arranged in an outermost peripheral region of the chip" and "serving to connect the other end of the first wiring to an I/O slot different from the first I/O slot," the semiconductor integrated circuit device of

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claim 1 enables an I/O slot requiring good characteristics (such as second I/O slot 11b, for example) to be connected to a pad having good characteristics (such as first pad 12a, for example) without changing a wiring pattern in an inner region of the chip. Thus, manufacturing costs can be reduced by using conventional masks on the chip uppermost level and the conventional built-up substrate of the package. The device of Janai does not realize these advantages of the present invention.

Further, Janai would not have motivated one of ordinary skill in the art to modify Applicants' so-called admitted prior art (Fig. 4) to result in the claimed invention, because Janai discloses fusing fusible links provided in an inner peripheral region of the chip. Particularly, Janai discloses a device including an array of semiconductor elements interconnected by fusible links. Fusing the links enables a particular function of the gate array device. However, before any links are fused, the circuit is inoperable. Thus, if Janai were modified so that fusible links M2 were provided only in "an outermost peripheral region of the chip," none of the semiconductor elements would be rendered operable. Accordingly, Janai provides no motivation or reasonable expectation of success for modifying Applicants' so-called admitted prior art to result in the claimed invention.

Because the Examiner provides insufficient evidence and reasoning as to why a skilled artisan having Applicants' so-called admitted prior art and Janai before him would have desired to make such a combination, the Examiner has not established a *prima facie* case of obviousness in rejecting claim 1 and the § 103(a) rejection of claim 1 should be withdrawn.

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The § 103(a) rejection of claims 6-8, 10 and 15-20 should be withdrawn as well, at least in view of their dependence from allowable claim 1.

CONCLUSION

In making the above references to the drawings and specification, it is to be understood that Applicants are in no way intending to limit the scope of the claims to the exemplary embodiments shown in the drawings and described in the specification. Rather, Applicants expressly affirm that they are entitled to have the claims interpreted broadly, to the maximum extent permitted by statute, regulation and applicable case law.

Attached hereto is a marked-up version of the changes made to the claims by this amendment. The attachment is captioned "**Appendix to the Amendment After Final of July 29, 2003**" Deletions appear as normal text surrounded by [ ] and additions appear as underlined text.

Applicants respectfully request that this Amendment under 37 C.F.R. § 1.116 be entered by the Examiner, placing claims 1, 6-8, 10 and 15-20 in condition for allowance. Applicants submit that the proposed amendment of claim 1 does not raise new issues or necessitate the undertaking of any additional search of the art by the Examiner, since all of the elements and their relationships claimed were either earlier claimed or inherent in the claims as examined. Therefore, this Amendment should allow for immediate action by the Examiner.

Furthermore, Applicants respectfully point out that the final action by the Examiner presented some new arguments as to the application of the art against Applicant's invention. It is respectfully submitted that the entering of the Amendment

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would allow the Applicants to reply to the final rejections and place the application in condition for allowance.

Finally, Applicants submit that the entry of the amendment would place the application in better form for appeal, should the Examiner dispute the patentability of the pending claims.

In view of the foregoing remarks, Applicants submit that this claimed invention, as amended, is neither anticipated nor rendered obvious in view of the prior art references cited against this application. Applicants therefore request the entry of this Amendment, the Examiner's reconsideration and reexamination of the application, and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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Dated: July 29, 2003

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APPENDIX TO AMENDMENT OF JULY 29, 2003

Version of Claims with Markings to Show Changes Made

AMENDMENTS TO THE CLAIMS:

Please amend claim 1, as follows:

1. (Amended Four Times) A semiconductor integrated circuit device, comprising:

first and second I/O slots arranged on the same wiring level in parallel along a peripheral portion of a chip within an inner region of the chip;

a first pad arranged on a wiring level different from said first I/O slot and arranged above the first I/O slot without being connected to the first I/O slot;

a second pad arranged on a wiring level different from said first I/O slot and arranged apart from the peripheral portion of the chip as compared with the first pad;

a first wiring comprising one end positioned in said first pad and comprising the other end positioned in the peripheral portion of the inner region of the chip above the first I/O slot;

a second wiring comprising one end positioned in the second pad and comprising the other end positioned in the peripheral portion of the inner region of the chip above the second I/O slot; and

a third wiring arranged in an outermost peripheral region of the chip and serving to connect the other end of the first wiring to an I/O slot different from the first I/O slot.

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